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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/840,244	04/23/2001	Didier Serra	1400.005	6527

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EXAMINER	
AU, SCOTT D	

ART UNIT	PAPER NUMBER
2635	7

DATE MAILED: 04/23/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/840,244	SERRA ET AL.	
	Examiner	Art Unit	
	Scott Au	2635	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *4/23/01*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2 and 11* is/are rejected.

7)☒ Claim(s) *3,4 and 7-10* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 April 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4,6*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

The application of Serra et al. for a "Contactless integrated circuit with reduced power consumption" filed April 23, 2001 has been examined.

Claims 1-11 are pending.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 1 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Silvian (US# 4,681,111).

Referring to claim 1, Silvian discloses a contactless integrated circuit (IC1) (2) (i.e. see the patient's transmitting device of Figures 1 and 4) comprising a device (LMC) (7) (i.e. tuned circuit) for modulating the load of an antenna coil (Ls) (4) (i.e. inductor), a device (CEC1) (11) (i.e. clock) for extracting a clock (H), and means (10) (i.e. shift register) for delivering a load modulation signal according to a binary signal to be transmitted (DTx) (i.e. signal A), characterized in that it comprises means (CC1) (22) (i.e. mode control selection switch) for delivering a pulsed load modulation signal (Slm4) comprising a series of load modulation pulses (I1-In), the duration of which is asynchronously calibrated by the charge or the discharge of at least one capacitor (38)

(Cas) (col. 5 lines 3-25 and 63-68, col. 8 lines 60-65 and col. 9 lines 1-17; see Figures 1 and 4). However, Silvian as silent on teaching a duration of which is asynchronously calibrated by the charge or the discharge of at least one capacitor.

Silvian discloses a R-C combination circuit is set to a fixed duration bit rate may be sent within an analog signal while transmitting in the digital mode and a R-C combination circuit is connected to a digital flip flop in order to create one-shot serial non-return zero data output signal.

One skilled in the art recognizes using a capacitor that connect to one shot multivibrator to connect in serial with a switch to generate charge or discharge output to a comparator in order to generate a duration of pulses output. Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention was made to use a capacitor connects to a digital flip flop to generate a serial data output in a duration of a charge and a discharge of capacitor in order to control a duration of a output signal.

Referring to claim 11, Silvian discloses Integrated circuit according to claim 1, wherein the means for inhibiting the clock extraction device (CEC1) comprise means (T5, T6) for powering-off the extraction device (CEC1) (col. 9 lines 52-68).

Claims 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Silvian (US# 4,681,111) as applied to claim 1 above, and further in view of Collins (US# 4,005,417).

Referring to claim 2, Silvian discloses an integrated circuit according to claim 1 above. However, Silvian did not explicitly disclose that it comprises means (WLCC, INV1, T5, T6) for inhibiting the clock (H) extraction device (CEC1) at least during the emission of the load modulation pulses.

In the same field of endeavor of inhibiting clock device, Collin discloses means (WLCC, INV1, T5, T6) (49) (i.e. inverter) for inhibiting the clock (H) extraction device (CEC1) at least during the emission of the load modulation pulses (col. 6 lines 40-61; see Figure 3) in order to transmit a pulse on line XMT to pulse modulator (14).

One of ordinary skilled in the art recognizes the need to have an inverter (49) to inhibits clock pulse from passing through selector (52) of Collin in the transmission and reception system of Silvian because Silvian suggests means for inhibiting the clock extraction device at least during the emission of the load modulation pulses in order to have an asynchronous operating periods. Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention was made to include inverter (49) for inhibiting the timing (15) device disclosed by Collins into inhibiting device of Silvian with the motivation for doing so would allow the operational system of the transmitter to operates in asynchronous or synchronous periods.

Claims 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Silvian (US# 4,681,111) as applied to claim 1 above, and further in view David Systems, INC. (EP# 299,639).

Referring to claim 6, Silvian discloses an integrated circuit according to claim 1 above. However, Silvian did not explicitly wherein the modulation signal (Slm4) is combined with an a.c. signal (Fsc) in order to form a load modulation signal comprising a.c. signal pulses.

In the same field of endeavor of combining signal, David System, INC. discloses wherein the modulation signal (Slm4) is combined with an a.c. signal (Fsc) in order to form a load modulation signal comprising a.c. signal pulses (col. 4 lines 38-44; see Figure 1) and producing a pulse for each transition of said modified frequency. modulation code.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention was made to include the modulation signal is combined with a communication medium in order to convert the data into modified frequency moduated code disclosed David System, INC. into system of Silvian with the motivation for doing so would allow the combined of signals to produce a load modulation signal.

Claim Objections

Claims 3-4 and 7-10 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Referring to claim 3, the following is a statement of reasons for the indication of

allowable subject matter: the prior art fail to suggest limitations that charging the first capacitor (Cref) with a constant current (Iref) before the emission of a load modulation pulse, during a time (Tref) fixed by a predetermined number of clock cycles (H), charging the second capacitor (Cas) with a constant current (Iref) during the emission of a pulse, and stopping the emission of the pulse when the charge voltage (Vas) of the second capacitor is equal to the voltage (Vref) at the terminals of the first capacitor.

Referring to claim 4, the following is a statement of reasons for the indication of allowable subject matter: the prior art fail to suggest limitations that transforming variation edges of the binary coded signal (S1) into load modulation pulses (I1-In) of short duration compared to the duration (Tb) of a bit of the binary signal to be transmitted (DTx).

Referring to claim 7, the following is a statement of reasons for the indication of allowable subject matter: the prior art fail to suggest limitations that wherein the load modulation pulses have a duration (Tas) shorter than or equal to the quarter of the duration of a bit of the binary signal to be transmitted (DTx).

Referring to claim 8, the following is a statement of reasons for the indication of allowable subject matter: the prior art fail to suggest limitations that wherein the clock extraction device (CEC1) is maintained in an inhibited state after the emission of a load modulation pulse, at least for a time (Tref, Tas) equal to the duration of a load modulation pulse.

Referring to claim 9, the following is a statement of reasons for the indication of allowable subject matter: the prior art fail to suggest limitations that wherein the clock

extraction device (CEC1) is arranged to extract a clock signal (H) from an a.c. voltage (Vac) induced in the antenna coil (Ls).

Referring to claim 10, the following is a statement of reasons for the indication of allowable subject matter: the prior art fail to suggest limitations that wherein the means for inhibiting the clock extraction device (CEC1) comprise means (T5, T6) for powering-off the extraction device (CEC1).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Goto (US# 5,889,273) discloses an IC card with clock extraction device.

Any inquiry concerning this communication or earlier communications form the examiner should be directed to Scott Au whose telephone number is (703) 305-4680. The examiner can normally be reached on Mon-Fri, 8:30AM – 5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Horabik can be reached at (703) 305-4704. The fax phone numbers for the organization where this application or proceeding is assigned are (703)-872-3906.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)-305-3900.

Scott Au

MICHAEL HORABIK
SUPERVISORY PATENT EXAMINER
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